ELECTRONICS FOR EXTREME ENVIRONMENTS: J.U. Patel[1], John. Cressler[2], Ying Li[2] and G. Niu[2], [1]Jet Propulsion Laboratory, 4800 Oak Grove Drive, Pasadena, CA 91109 m/s 303-310 jupatel@jpl.nasa.gov, [2]The Electrical Engineering Department, Auburn University, Auburn, Alabama, 36849.

Introduction: Most of the NASA missions involve extreme environments comprising radiation and low or high temperatures. Current practice of providing friendly ambient operating environment to electronics costs considerable power and mass (for shielding). Immediate missions such as the Europa orbiter and lander and Mars landers require the electronics to perform reliably in extreme conditions during the most critical part of the mission. Some other missions planned in the future also involve substantial surface activity in terms of measurements, sample collection, penetration through ice and crust and the analysis of samples. Thus it is extremely critical to develop electronics that could reliably operate under extreme space environments.

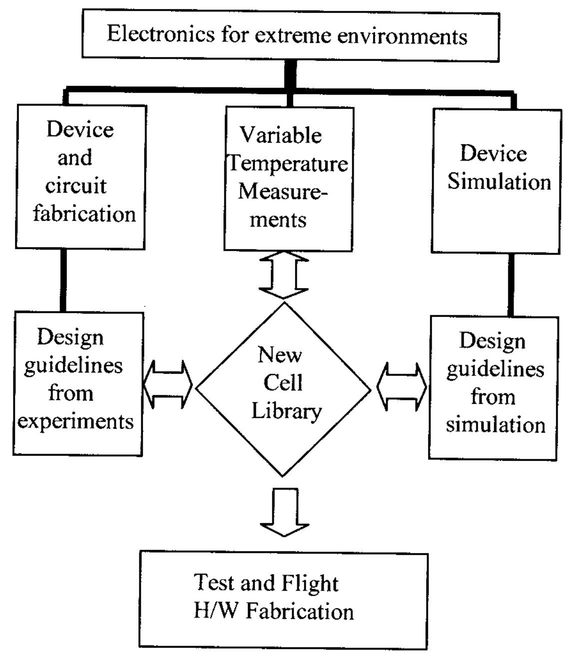
Silicon On Insulator (SOI) technology is an extremely attractive candidate for NASA's future low power and high speed electronic systems because it offers increased transconductance, decreased sub-threshold slope, reduced short channel effects, elimination of kink effect, enhanced low field mobility and immunity from radiation induced latch-up. A common belief that semiconductor devices function better at low temperatures is generally true for bulk devices but it does not hold true for deep sub-micron SOI CMOS devices with microscopic device features of 0.25 μm and smaller. Various temperature sensitive device parameters and device characteristics have recently been reported in the literature. Behavior of state of the art technology devices under such conditions needs to be evaluated in order to determine possible modifications in the device design for better performance and survivability under extreme environments.

Here, we present a unique approach of developing electronics for extreme environments to benefit future NASA missions as described above. This will also benefit other long transit/life time missions such as the solar sail and planetary outposts in which electronics is out open in the unshielded space at the ambient space temperatures and always exposed to radiation.

Technical approach: Developing electronics for extreme environments involve; a. characterization of current SOI technologies in extreme environments, b. determination of the device design modification for a better survivability and reliable operation in extreme environments , c. formulation of cell libraries with modified device designs and d. design, fabrication and testing of electronics using modified cell libraries. This will be accomplished with the following steps:

- Experimental characterization of state-of-the-art SOI CMOS technologies (0.25 μm and smaller) in low temperature (77K to 300K) and radiation environments (300-1000 Krads protons and gamma).
- Theoretical simulation of the same devices under similar conditions using the device simulator DESSIS to verify experimental results and determine the temperature and radiation sensitive device features. Critical features will include shapes of the source and drain structures, doping profiles, oxide thickness, channel length etc.
- Determine necessary modifications in the device design and architecture using device simulator DESSIS in order to minimize sensitivity to the combined environment of low temperature and radiation. Formulate new device design guidelines and cell libraries based upon the modifications.

Fabricate basic electronics circuits such as op-amp and sense-amps using modified cell libraries.



Results from the initial characterization of current technologies are expected to be immediately useful in determining radiation and tolerance temperature of current electronics for designing the spacecraft shielding, temperature and in the planning of other mission activities.

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